1. A camouflaged interconnection scheme for interconnecting two spaced-apart implanted regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising:

a first implanted region in the integrated circuit or device forming a conducting channel between two spaced-apart implanted regions, the conducting channel being of said common conductivity type and bridging a region between said two spaced-apart implanted regions; and

a second implanted region of opposite conductivity type in the integrated circuit or device, said second implanted region being disposed between said two spaced-apart implanted regions of common conductivity type and overlying said conducting channel.

2. The invention of claim 1 wherein said second implanted region overlying said conducting channel has a larger area, when viewed in a direction normal to a major surface of the integrated circuit or device, than has said conducting channel.

3. The invention of claim 1 wherein said two spaced-apart implanted regions form source and/or drain contacts, respectively, of two separate field effect transistors (FETs).

4. The invention of claim 1 wherein the second implanted region is provided in said integrated circuit or device over regions having no conducting channels formed therein.

5. A camouflaged interconnection scheme for interconnecting a plurality of spaced-apart implanted regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising:

a plurality of interconnects each interconnecting selected implant regions of said plurality of spaced-apart implanted regions, each interconnect comprising a buried conducting channel bridging a region between the selected implant regions; and

at least one implanted region of opposite conductivity type in the integrated circuit or device, the at least one implanted region of opposite conductivity type being

disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects.

6. The invention of claim 5 wherein said at least one implanted region of opposite conductivity type has a larger area than a total area of a related at least one of said conducting channels, when viewed in a direction normal to a major surface of the integrated circuit or device.

7. The invention of claim 5 wherein at least selected one of said spaced-apart implanted regions form source and/or drain contacts, respectively, of adjacent field effect transistors (FETs).

8. The invention of claim 5 wherein the at least one implanted region of opposite conductivity type is provided in said integrated circuit or device over regions having no conducting channels formed therein.

15. An interconnection scheme for interconnecting two spaced-apart regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising:

a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type, the first region providing a buried conducting channel for the two spaced-apart regions; and

a second region of opposite conductivity type in the integrated circuit or device, said second region overlaying said first region to conceal the conducting channel.

16. The interconnection scheme of claim 15 wherein said second region overlying said first region has a larger area, when viewed in a direction normal to a major surface of the integrated circuit or device, than has said first region.

17. The interconnection scheme of claim 15 wherein said two spaced-apart regions form source and/or drain contacts, respectively, of two separate field effect transistors (FETs).

18. An interconnection scheme for interconnecting two spaced-apart regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising:

a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type, the first region providing a buried conducting channel for the two spaced-apart regions;

a second region of opposite conductivity type in the integrated circuit or device, said second region overlaying said first region to conceal the conducting channel;

at least one additional spaced-apart region of the common conductivity type, said at least one additional spaced-apart region being spaced apart from the two spaced-apart regions; and

at least one additional region of the opposite conductivity type is provided in said integrated circuit or device, said at least one additional region being disposed laterally of and in direct contact with one of the two spaced-apart regions and the at least one additional spaced-apart region of the common conductivity type, wherein the one of the two spaced-apart regions and the at least one additional spaced-apart region do not have the buried conducting channel formed therebetween.

19. A interconnection scheme for interconnecting a plurality of spaced-apart regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising:

a plurality of buried conducting channels, each buried conducting channel being of the common conductivity type, each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions, each buried conducing channel providing an electrical connection between said selected ones of the plurality of spaced-apart regions; and

at least one region of an opposite conductivity type in the integrated circuit or device, the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels.

20. The interconnection scheme of claim 19 wherein said at least one region of opposite conductivity type has a larger area than a total area related to at least one of said buried conducting channels, when viewed in a direction normal to a major surface of the integrated circuit or device.

21. The interconnection scheme of claim 19 wherein at least selected ones of said spaced-apart regions form source and/or drain contacts, respectively, of adjacent field effect transistors (FETs).

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22. (Once Amended) The interconnection scheme of claim 19 further comprising at least one other region of the opposite conductivity type, the at least one other region of the opposite conductivity type being laterally disposed of and in direct contact with additional selected ones of the plurality of spaced-apart regions, wherein said additional selected ones of the plurality of spaced-apart regions are not electrically connected by one of said plurality of buried conducting channels.

23. (New) The invention of claim 1 wherein the second implanted region has a depth less than a depth of the first implanted region.

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24. (New) The invention of claim 5 wherein the at least one implanted region of opposite conductivity type has a depth less than a depth of each of said plurality of interconnects.

25. (New) The invention of claim 15 wherein the second region of opposite conductivity type has a depth less than a depth of said first region.

26. (New) The invention of claim 19 wherein the at least one region of opposite conductivity type has a depth less than a depth of each of said plurality of buried conducting channels.